RG

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,381	08/17/2001	Serge Lasserre	TI-31354	4434

23494 7590 04/26/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	PAPER NUMBER
2188	14

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,381	LASSERRE, SERGE	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-6* is/are allowed.

6)☒ Claim(s) *1,2 and 11-13* is/are rejected.

7)☒ Claim(s) *7-10 and 14-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 15 March 2004 has been considered. Please see the attached PTO-1449(s).

Specification

2. Applicant is requested to update any data (continuation serial number, patent number, etc...) concerning co-pending or related applications listed in the specification.

The status of the parent applications on pages 1 and 11 should be updated as appropriate.

Claim Objections

3. Claims 7-10 and 14-20 are objected to because of the following informalities:

As per claim 7, lines 8, 11, and 12 (both instances), "valid" should be --dirty--.

As per claim 14, line 2, "the address" should be --an address--.

As per claim 17, line 6, --the selected segment-- should be added after "that".

As per claim 18, line 4, --dirty state-- should be --set state--.

As per claim 19, line 10, --the-- should be added before "step".

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baron et al. in view of Tanenbaum ("Modern Operating Systems").

As per claims 1 and 12, Baron et al. teaches an IC chip including a processor 4 and a memory ("local memory") 10, where the memory occupies at least a portion of the address space of the processor (i.e. the memory is not a cache memory exclusively). The memory includes 8 sectors ("plurality of segments") of 128 words each. See column 4, lines 45-53. Each word in each sector is associated with a valid bit ("plurality of indicator bits"). See column 5, lines 1-9. The IC chip can operate in a PRAM mode of operation (i.e. non-cache mode of operation). See column 4, lines 39-42. When operating in the PRAM (or STANDARD) mode of operation direct memory access (DMA) transfers occur between the program memory and the external memory using a DMA controller ("DMA circuitry"). See column 59-63. Even when operating in the PRAM mode, the valid bits are set by the DMA transfer ("operable to manipulate a selected portion of indicator bits...corresponding to the selectable portion of segments"). See column 8, lines 31-35.

Baron et al. teaches that the valid bits are used by the processor, and therefore teaches the limitations of "address circuitry, for controlling access by the first processor to the addressed location of the local memory within the address space and responsive to the state of the indicator

bits corresponding to the addressed location" (claim 1) or "controlling access by the processor to the first segment in the local memory within the address space, responsive to the state of the first indicator bit" (claim 12). Note figure 2, where the valid bits for a sector are connected to the "hit/miss" circuitry. See also column 5, lines 1-9 and 42-56, where the use of the valid bits is described in relation to the cache operation.

Baron et al. does not teach the specifics of the DMA transfer, in particular that the controller transfers a selectable portion of segments from a selectable region of the external memory. Tanenbaum teaches DMA transfers where the CPU gives the DMA controller three items of information for the DMA transfer: the disk (i.e. external) address of the desired data ("selectable region of a second memory"), the internal memory address where the desired data is to be placed, and the number of bytes to transfer ("selectable portion of segments"). See the first full paragraph on page 209 (lines 7-9). It would have been obvious to one of ordinary skill in the art to have implemented the standard DMA transfer operation, as taught by Tanenbaum, in the system of Baron et al., because Tanenbaum teaches that this procedure frees the CPU from low-level work, thereby allowing the CPU to more efficiently use its time. See page 209, lines 5-7.

As per claims 2 and 13, Baron et al. teaches that the plurality of bits are valid bits set by the DMA controller during a DMA transfer as detailed above for claims 1 and 12. It the valid bit is not set, then a cache miss is indicated as detailed above, thereby not permitting the processor to access the data.

6. Claims 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (6,643,713) in view of Baron et al. in further view of Tanenbaum ("Modern Operating Systems").

Nakagawa et al. teaches a digital cellular telephone specification that includes (with reference to figure 2), a keyboard 235, a liquid crystal device 237 ("display"), RF modem 210, and an antenna 213. The CPU 227 and DSP chip 223 are connected to the LCD and keyboard over bus 229, the RF modem is indirectly connected to the DSP chip and the CPU, and the antenna is indirectly connected to the RF modem. Nakagawa et al. further teaches a DSP/CPU integrated chip with a cache and DMA controller. See figure 7.

Nakagawa et al. does not teach that internal cache RAM of figure 7 includes a plurality of indicator bits, or that the DMA circuitry (see element 705 in figure 7) is operable to transfer a selectable portion of segments of the plurality of segments from a selectable region of a second memory and operable to manipulate a selected portion of indicator bits...corresponding to the selectable portion of segments.

Baron et al. teaches an IC chip including a processor 4 and a memory ("local memory") 10, where the memory occupies at least a portion of the address space of the processor (i.e. the memory is not a cache memory exclusively). The memory includes 8 sectors ("plurality of segments") of 128 words each. See column 4, lines 45-53. Each word in each sector is associated with a valid bit ("plurality of indicator bits"). See column 5, lines 1-9. The IC chip can operate in a PRAM mode of operation (i.e. non-cache mode of operation). See column 4, lines 39-42. When operating in the PRAM (or STANDARD) mode of operation direct memory access (DMA) transfers occur between the program memory and the external memory using a DMA controller ("DMA circuitry"). See column3, lines 59-63. Even when operating in the PRAM mode, the valid bits are set by the DMA transfer ("operable to manipulate a selected

portion of indicator bits...corresponding to the selectable portion of segments"). See column 8, lines 31-35.

It would have been obvious to one of ordinary skill in the art to have modified Nakagawa et al. to replace the DSP/CPU integrated chip with the DSP chip of Baron et al. because Baron et al. teaches at column 1, lines 38-39, that such a chip would provide an optimum use of silicon area.

The combination of Nakagawa et al. and Baron et al. does not teach the specifics of the DMA transfer, in particular that the controller transfers a selectable portion of segments from a selectable region of the external memory. Tanenbaum teaches DMA transfers where the CPU gives the DMA controller three items of information for the DMA transfer: the disk (i.e. external) address of the desired data ("selectable region of a second memory"), the internal memory address where the desired data is to be placed, and the number of bytes to transfer ("selectable portion of segments"). See the first full paragraph on page 209 (lines 7-9). It would have been obvious to one of ordinary skill in the art to have implemented the standard DMA transfer operation, as taught by Tanenbaum, because Tanenbaum teaches that this procedure frees the CPU from low-level work, thereby allowing the CPU to more efficiently use its time. See page 209, lines 5-7.

1. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blumrich et al.

As per claim 20, Blumrich et al. does not teach a mode circuit which in one mode transfers only dirty segments and in another mode transfers the entire block. However it would have been obvious to one of ordinary skill in the art to have modified Blumrich et al. to incorporate a mode circuit such that in one mode transfers only dirty segments and in another

mode transfers the entire block because this would increase the flexibility of the system. Blumrich et al. already teaches transferring to memory only dirty blocks. Incorporating the ability to transfer plural blocks without referring to the main memory would permit fast cache flushing on context changes.

Allowable Subject Matter

2. Claims 3-6 are allowed.

3. Claims 7-10 and 14-20 are allowable over the prior art of record, but are objected to as set forth above.

Response to Arguments

4. Applicant's arguments filed 15 March 2004 have been fully considered but they are not persuasive.

With respect to Applicant's arguments concerning claim 11, and the applicability of the Nakagawa et al. reference, Applicant is clearly incorrect. Nakagawa et al. has the benefit of filing date of the 09/051,286 application in accordance with 35 U.S.C §120, which is prior to the filing date of the present application.

With respect to Applicant's arguments concerning the combination of Baron et al. and Tanenbaum, these are not persuasive. Applicant argues that the teaching of column 8, lines 36-39, indicates that the processor does not use the valid bits and therefore does not teach the limitation of "address circuitry, for controlling access by the first processor to the addressed location of the local memory within the address space and responsive to the state of the indicator

bits corresponding to the addressed location" (claim 1) or "controlling access by the processor to the first segment in the local memory within the address space, responsive to the state of the first indicator bit" (claim 12). However, the section cited by Applicant only teaches not using the valid bits in the PRAM mode. In the CACHE mode the valid bits are used by the processor for controlling access by the processor to the cache. Note figure 2, where the valid bits for a sector are connected to the "hit/miss" circuitry. See also column 5, lines 1-9 and 42-56, where the use of the valid bits is described in relation to the cache operation.

Therefore, Baron et al. teaches that the valid bits are used by the processor, and therefore teaches the limitations of "address circuitry, for controlling access by the first processor to the addressed location of the local memory within the address space and responsive to the state of the indicator bits corresponding to the addressed location" (claim 1) or "controlling access by the processor to the first segment in the local memory within the address space, responsive to the state of the first indicator bit" (claim 12).

Conclusion

5. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
April 26, 2004